Amendments to the Claims:

Please amend the claims as set forth below.

1. (Original) A method of reinserting Vertical Blanking Interval data in a digital video signal comprising;

creating a gray scale palette in an On Screen Display memory;

sizing a Vertical Blanking Interval area in an On Screen Display memory;

locating a Vertical Blanking Interval area in an On Screen Display memory;

generating a Vertical Blanking Interval luma waveform bitmap; and

overlaying said Vertical Blanking Interval luma waveform bitmap in a digital video signal according to the gray scale palette, size and location data stored in the On Screen Display memory.

2. (Original) The method of claim 1 wherein said gray scale palette is stored between uses.

3. (Original) The method of claim 1 wherein size data is stored between uses.

4. (Original) The method of claim 1 wherein said location data is stored between uses.

5. (Original) The method of claim 1 wherein said digital video signal is an uncompressed signal from a digital video-broadcasting bitstream.

6. (Original) The method of claim 1 wherein said overlaying step is by summing a Vertical Blanking Interval luma waveform with the digital video signal.

7. (Original) The method of claim 1 wherein said video bitstream is configured according to MPEG protocols.

8. (Currently Amended) An On Screen Display processor for reinserting Vertical Blanking Interval data in a digital video signal comprising:

an On Screen Display controller;

a Vertical Blanking Interval waveform builder module configured to create a ~~video~~ Vertical Blanking Interval Data bitmap;

an On Screen Display memory, said On Screen Display memory being configured to retain Vertical Blanking Interval position data, Vertical Blanking Interval size data and a Vertical Blanking Interval gray scale palette;

said On Screen Display controller being configured to receive the Vertical Blanking Interval waveform bitmap from said Vertical Blanking Interval waveform builder module and insert the Vertical Blanking Interval waveform bitmap into a digital video signal in operative communication with said On Screen Display controller, according to the position, size and gray scale data stored in said On Screen Display region memory.

9. (Original) The processor of claim 8 wherein said Video Blanking Interval Data gray scale palette remains stored in said On Screen Display memory between uses.

10. (Original) The processor of claim 8 wherein the Vertical Blanking Interval Data position data remains stored in said On Screen Display memory between uses.

11. (Original) The processor of claim 8 wherein the Vertical Blanking Interval Data size data remains stored in said On Screen Display memory between uses.

12. (Original) The processor of claim 8 wherein said On Screen Display Controller is configured to insert the Vertical Blanking Interval waveform bitmap by summing said waveform bitmap with the digital video signal.

13. (Original) The processor of claim 8 wherein the video bitstream into which the On Screen Display processor inserts the Vertical Blanking Data is configured according to MPEG protocols.

14. (New) The processor of claim 8 wherein said video blanking interval grayscale palette is regenerated for each use.

15. (New) The processor of claim 8 wherein said video blanking interval position data is regenerated for each use.

16. (New) The processor of claim 8 wherein said video blanking interval size data is regenerated for each use.

17. (New) The processor of claim 8 further comprising an input buffer in operative communication with said Vertical Blanking Interval waveform builder.

18. (New) The processor of claim 8 further comprising an output buffer in operative communication with said Vertical Blanking Interval waveform builder.

19. (New) The processor of claim 8 further comprising separate input buffers for even and odd fields, each of said input buffers being in operative communication with said Vertical Blanking Interval waveform builder.

20. (New) The processor of claim 8 further comprising an integrated receiver and decoder in which said On Screen Display processor is operatively deployed.

21. (New) The processor of claim 8 wherein said Vertical Blanking Interval wavefrom builder is embodied in a separate microprocessor adapted for operative communication with a processor processing media content data streams.

22. (New) The processor of claim 8 wherein said On Screen Display controller is configured to add ancillary wave forms.

23. (New) The processor of claim 22 wherein said On Screen Display controller is configured to add clock run in preambles.

24. (New) The processor of claim 8 further comprising at least one additional memory region, each additional memory region being configured to retain said Vertical Blanking Interval position data, said vertical blanking interval size data, and said Vertical Blanking Interval grayscale palette.

25. (New) The processor of claim 24 wherein further comprising at least one first memory region for even fields and at least one second memory region for odd fields.

26. (New) The processor of claim 8 wherein said grayscale palette allocates eight bytes per pixel.

27. (New) The processor of claim 8 further comprising a digital video serializer in operative communication with a digital video output, said digital video output receiving the output of said On Screen Display controller.

28. (New) The processor of claim 8 wherein Vertical Blanking Interval data is displayed according to a screen space size defined at a single Vertical Blanking Interval data region.

29. (New) The processor of claim 8 wherein Vertical Blanking Interval data is displayed according to a first Vertical Blanking Interval data size region for an even field and a second Vertical Blanking Interval data size region for an odd field.

30. (New) The processor of claim 29 wherein each separate Vertical Blanking Interval data region has a separate grayscale palette.

31. (New) The processor of claim 8 wherein said Vertical Blanking Interval bitmap is further configured to skip every other line on an even field and skip alternate lines on an odd field.

32. (New) The processor of claim 8 wherein said Vertical Blanking Interval waveform builder writes a bitmap to an even field memory region during the same clock cycle as an odd field memory region is read from memory.

33. (New) A data structure comprising:

a gray scale palette in an On Screen Display memory;

a Vertical Blanking Interval size in an On Screen Display memory;

a Vertical Blanking Interval position in an On Screen Display memory;

a Vertical Blanking Interval luma waveform bitmap; and

a Vertical Blanking Interval luma waveform bitmap overlay algorithm configured to overlay said Vertical Blanking Interval luma waveform bitmap in a digital video signal according to said gray scale palette, size and location data stored in said On Screen Display memory.

34. (New) A Vertical Blanking Interval data insertion system comprising:

a memory configured to store a gray scale palette, a Vertical Blanking Interval size, a Vertical Blanking Interval position;

a Vertical Blanking Interval luma waveform bitmap generator in operative communication with a transport data stream processor and in operative communication with said memory; and

an On Screen Display Processor configured to overlay said Vertical Blanking Interval luma waveform bitmap in a digital video signal according to the gray scale palette, size and location data stored in the On Screen Display memory.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

By: Robert C. Haldiman
Husch & Eppenberger, LLC
190 Carondelet Plaza
St. Louis, MO 63105
309-637-4900
309-637-4928 FAX